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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,657	10/01/2003	Stanley N. Protigal	2269-2898.4US (88-0070.09	8993

24247 7590 03/22/2005

TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,657	PROTIGAL ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/2004 & 3/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujii ("Fujii") USPN 4,654,689.

Fujii discloses in figs. 5 and 6 a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising: a carrier substrate; and a semiconductor device secured and operably coupled to the carrier substrate and including: a semiconductor substrate 10 having active circuit devices 20 thereon; and an on-chip capacitor (51, 55 and 52) including at least a portion thereof being formed in an active area of the semiconductor substrate underlying at least two bus signals (11/12, 13) of the active circuit devices, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian et al. ("Kazerounian") USPN 5,014,097.

Kazerounian discloses (figs. 2-8 and col. 7, lines 57-68) a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system

comprising: a carrier substrate; and a semiconductor device secured and operably coupled to the carrier substrate and including: a semiconductor substrate 257/422 having active circuit devices 101/400 thereon; and an on-chip capacitor 110 including at least a portion thereof being formed in an active area of the semiconductor substrate underlying at least two bus signals (Vpp, Vout) of the active circuit devices, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

4. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujii.

Fujii discloses in figs. 5 and 6 a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising: a semiconductor substrate 10; active circuit devices 20 on the semiconductor substrate; and a capacitor (51, 55 and 52) having at least a portion thereof formed in an active area of the semiconductor substrate underlying at least two bus signals (11/12, 13) of the active circuit devices, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device when the semiconductor device is operably connected to the carrier substrate.

5. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian.

Kazerounian discloses (figs. 2-8 and col. 7, lines 57-68) a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising: a semiconductor substrate 257/422; active circuit devices 101/422 on the semiconductor substrate; and a capacitor 110 having at least a portion thereof formed in an active area of the semiconductor substrate underlying at least two bus signals (Vpp, Vout) of the active circuit devices, the capacitor being operably coupled to the active circuit devices to provide filtering

capacitance for the semiconductor device when the semiconductor device is operably connected to the carrier substrate.

6. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujii.

Fujii discloses in figs. 5 and 6 a semiconductor die assembly configured for connection to external circuitry, the semiconductor die assembly comprising: a carrier substrate configured for providing power and ground for at least one semiconductor die operably connected thereto; and at least one semiconductor die operably connected to the carrier substrate and including: a semiconductor substrate 10 having active circuit elements 20 formed on an active area thereof; and at least one capacitor (51, 55 and 52) on the semiconductor substrate underlying at least two bus signals (11/12, 13) of the active circuit elements, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor being operably coupled to the active circuit elements to provide filtering capacitance for the at least one semiconductor die.

7. Claim 3 is rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian.

Kazerounian discloses (figs. 2-8 and col. 7, lines 57-68) a semiconductor die assembly configured for connection to external circuitry, the semiconductor die assembly comprising: a carrier substrate configured for providing power and ground for at least one semiconductor die operably connected thereto; and at least one semiconductor die operably connected to the carrier substrate and including: a semiconductor substrate 257/422 having active circuit elements 101/422 formed on an active area thereof; and at least one capacitor 110 on the semiconductor substrate underlying at least two bus signals (Vpp, Vout) of the active circuit elements, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor

being operably coupled to the active circuit elements to provide filtering capacitance for the at least one semiconductor die.

8. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Fujii.

Fujii discloses (figs. 5-6 and abstract) a semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising: a semiconductor substrate having active circuit elements 20 formed on an active area thereof; at least one capacitor (51, 55 and 52) on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area underlying at least two bus signals (11/12, 13) of the active circuit elements, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefore when the semiconductor device is operably connected to power and ground of the carrier substrate.

9. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Kazerounian.

Kazerounian discloses (figs. 2-8 and col. 7, lines 57-68) a semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising: a semiconductor substrate having active circuit elements 101/422 formed on an active area thereof; at least one capacitor 110 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area underlying at least two bus signals (Vpp, Vout) of the active circuit elements, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefore when the semiconductor device is operably connected to power and ground of the carrier substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 28

ANS
March 15, 2005